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HARDWARE AND SOFTWARE FOR NUCLEAR SPECTROSCOPY ON THE VARIAN DATA MACHINES 622/i COMPUTER

by

C. E. Cohn, E. F. Bennett,
and T. J. Yule

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Applied Physics Division

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TABLE OF CONTENTS

LIST OF FIGURES

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ABSTRACT

A Varian Data Machines 622/i Computer has been interfaced with a dual analog-digital converter (ADC) and a display oscilloscope for use as a pulse-height-analysis system. Two binary counters have also been provided as general-purpose input channels. This report describes the interfaces and a representative machine-language pulse-height-analysis program.

INTRODUCTION

A Varian Data Machines 622/i Computer (i.e., the 18-bit version of the 16-bit 620/i) with 8K memory has been set up for on-line pulse-height analysis through interfacing to a Northern Scientific NS-625 dual ADC and a display oscilloscope. Programs for using these facilities have been prepared. A pair of general-purpose binary counters has been included. (With a few minor exceptions, the designs and programs can be used without change for the 620/i.) The 18-bit machine has been found superior to the 16-bit version for these applications, because the maximum count that can be stored in 16 bits is inconveniently small. The system has been used for fast-neutron spectroscopy by proton-recoil proportional counting.[1] This report describes the hardware and software in sufficient detail to allow duplication and use by interested parties.

Since the interfaces were built, improved components have become available in some instances. These will be noted where applicable.

The interfaces were implemented with Motorola resistor-transistor-logic (MRTL) integrated circuits. (At present, the prices of DTL and TTL circuits have declined sufficiently to make them attractive alternatives.) To understand the operation of the MRTL circuits, it is necessary, first of all, to remember the rule that the output of a gate is high if and only if all inputs are low. An inverter, whose symbol is shown in Fig. 1, is equivalent to a gate with one input. Other aspects will be discussed in due course. The circuits are powered by a 3.6-V supply included in the interface.

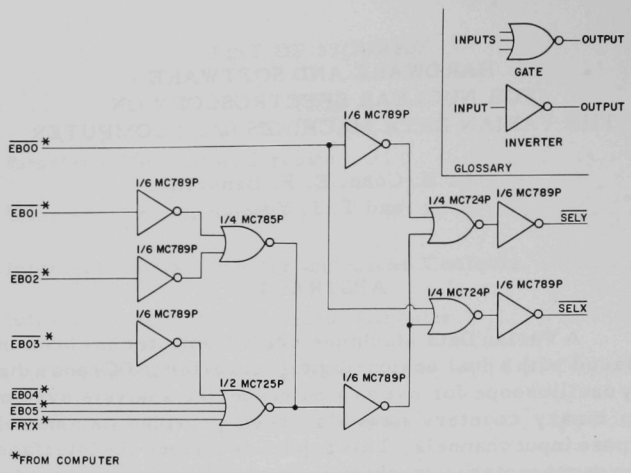

Fig. 1. ADC Interface: Selection Circuits. ANL Neg. No. 116-159.

COMPUTER INTERFACE CONSIDERATIONS

The 622/i communicates with external devices via a parallel bus, 18 bits wide, known as the E-bus. This bus carries both data and control codes, and is supplemented with a number of additional control lines. Each of these lines is high to indicate logic-zero or false, and is low to indicate logic-one or true. (Such an assignment of states is indicated by a bar over the signal designation.) Thus, a logic-one signal may be impressed on any line by shorting it to ground.

The status of the E-bus is indicated by two of the auxiliary lines, known as Function Ready ($\overline{\text{FRYX}}$) and Data Ready ($\overline{\text{DRYX}}$). Whenever the computer communicates with an external device, $\overline{\text{FRYX}}$ is pulsed low for 0.45 μsec. During this interval, the low-order six bits of the E-bus (lines EB00 through EB05) carry the device address, while the higher-order lines indicate the operation being performed. If the operation is an input or an output, $\overline{\text{DRYX}}$ is also pulsed low for 0.45 μsec, starting 1.35 μsec after the termination of $\overline{\text{FRYX}}$. For an output operation, the output data will appear on the E-bus while $\overline{\text{DRYX}}$ is low. For an input operation, the external device must place its data on the E-bus during the same interval.

The various external devices are connected to these lines via a "party-line" cable, which starts at the computer and runs from device to device. Each line is terminated by a 150-ohm resistor to the supply voltage at each end of the cable. This supply voltage is maintained at 2.8 V by an emitter follower in the computer with a Zener diode in its base circuit.

However, the computer itself communicates with the E-bus through diode-transistor logic (DTL) circuits supplied with 5 V. Thus, the much lower party-line supply voltage is very close to the logic thresholds in the DTL circuits. A slight amount of loading on a line can pull the logic-zero voltage down sufficiently that it will not be recognized by the computer. This difficulty was partly ameliorated by connecting the supply wire of the party line to the 3.6-V supply used for the interface logic circuits. This cuts off the emitter follower in the computer, so that all the interface circuits are supplied with this higher voltage from the external supply. Nevertheless, the loading effect of the RTL input circuits still brought some of the lines down to where operation was marginal. Therefore, the input circuits were isolated from the lines through emitter followers. Each emitter follower uses one 2N3904 NPN transistor. The collector of the transistor was connected to the supply voltage, the base to the line involved, and the emitter to all the RTL circuits driven by that line. Each interface has an emitter follower on every line from which it receives signals. These are not shown on the diagrams.

ADC INTERFACE

The ADC interface provides for transmission of data from the Northern Scientific NS-625 dual ADC to the computer on command, and clears the data from the dual ADC when the transfer is complete. When interrogated by the computer via a sense instruction, it indicates whether either ADC has data ready to be read.

The X and Y ADC's have been assigned device addresses 61_8 and 60_8, respectively. These addresses are detected by the circuits shown in Fig. 1. If either address appears on the E-bus in coincidence with FRYX, then Select X ($\overline{\text{SELX}}$) or Select Y ($\overline{\text{SELY}}$), respectively, will become true.

The circuits in Fig. 2 indicate to the computer whether either ADC has data to be read. When either ADC is holding data, its corresponding STORE signal goes to +6 V. Since such a signal, higher than the supply voltage, cannot be safely applied to an RTL input, an emitter follower is inserted to hold the signal to a safe level. If the device address of one of the ADC's appears on the E-bus in coincidence with FRYX, if E-bus line 12 is simultaneously low (indicating a sense instruction), if the STORE signal from that ADC is high, and if the coincidence condition discussed below is fulfilled, then all inputs to one of the four-input gates will be low and its output will be high, turning on the associated transistor. This produces a positive response to the sense instruction by grounding the Sense Response ($\overline{\text{SERX}}$) line.

In two-parameter analysis, the STORE signals from both ADC's should be high after an event has been processed. However, an overflow

in one ADC will drop out its STORE signal and leave the other one high. Such an occurrence would lead to incorrect readings. Therefore, those events must be rejected. This is done by comparing the two STORE signals in a half adder. If one STORE signal is high and the other is low, the output of the half adder (labeled RESET) will be high. This inhibits the four-input gates and generates an immediate reset for the ADC, as will be described later. In one-parameter analysis, it is permissible for one STORE signal to be high while the other is low, since the two ADC's work independently. In that mode, the half adder is disabled by manually grounding the RESET line via Section A of the DPDT switch S1.

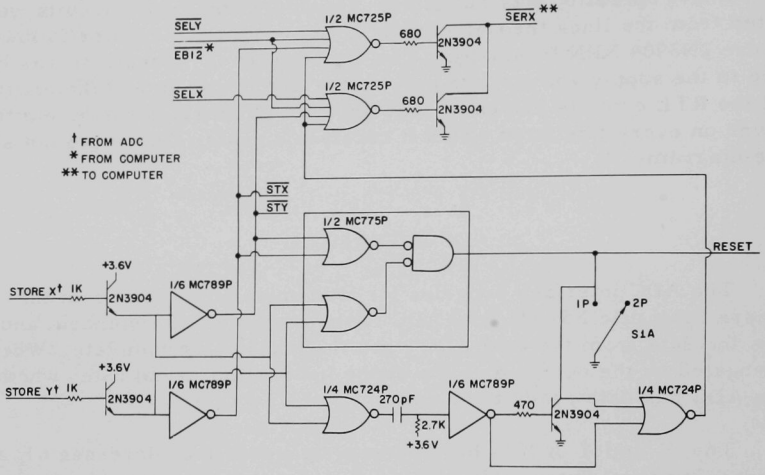

Fig. 2. ADC Interface: Ready Sensing. ANL Neg. No. 116-154.

Because of circuit delays in the ADC, the two STORE signals do not arrive simultaneously. Rather, one may precede the other by up to 1 μsec. To prevent a false RESET signal from being thus developed, the RESET line is held grounded for about 1.5 μsec after the first STORE signal arrives, and the development of a ready response is inhibited during this time.

Figure 3 shows the circuits that control the transfer of data from the ADC to the computer and the subsequent clearing of the ADC. An input operation, for example from the X-ADC, begins with $\overline{\text{SELX}}$ becoming low in synchronism with $\overline{\text{FRYX}}$. At the same time, E-bus line 13 is low, indicating that a data-input transfer is to be performed. This combination places positive signals on the set (S) and clock (T) inputs of the ENABLE X flip-flop. This primes the flip-flop to be set. When $\overline{\text{SELX}}$ goes high at the termination of $\overline{\text{FRYX}}$, these inputs drop to ground, setting the flip-flop.

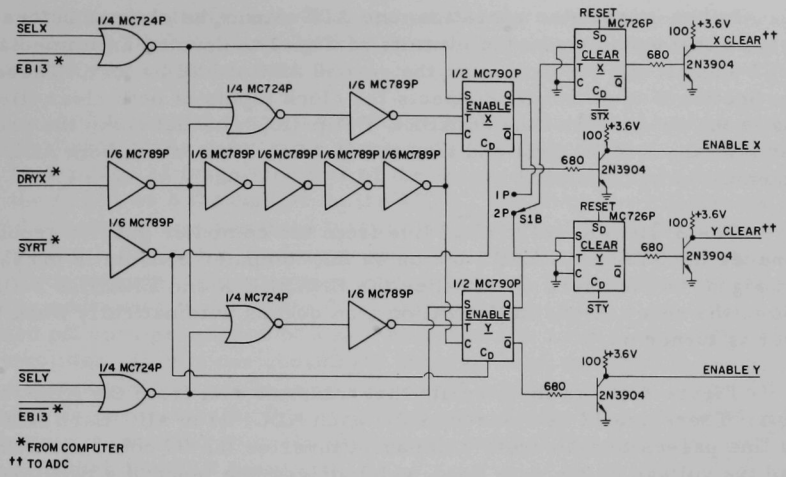

Fig. 3. ADC Interface: Data Transfer and Clear Controls. ANL Neg. No. 116-156.

The set output terminal, Q, goes high, while the reset output terminal, $\overline{Q}$, goes low. The set output is connected to the clock input of the CLEAR X flip-flop, priming it for a change of state. Since the latter is initially reset, the transition will be to the set state. The reset output terminal causes the ENABLE X line to go high, causing the ADC data to be placed on the E-bus, as will be described later.

Then $\overline{\text{DRYX}}$ goes low while the computer reads the data on the E-bus. While $\overline{\text{DRYX}}$ is low, a positive voltage is applied to the clock and reset (C) inputs on the ENABLE X flip-flop. This primes the flip-flop to be reset. After the computer has finished reading the data, $\overline{\text{DRYX}}$ goes high and the flip-flop resets. (The four inverters in series in the reset-input circuit do not perform any logical function, but were provided to adjust the propagation delays at the clock and reset inputs to ensure that C will remain high until T goes low, for reliable resetting.)

The reset output of the flip-flop goes high, dropping the ENABLE X signal to ground and removing the data from the E-bus. Meanwhile, the set output goes low, setting the CLEAR X flip-flop. This makes the X CLEAR signal high, clearing the ADC. When the clear operation is complete, the STORE signal from the ADC will go to ground. This makes the $\overline{\text{STX}}$ signal high, resetting the CLEAR X flip-flop. If the coincidence condition is violated, the CLEAR X flip-flop will be set by the RESET signal described above and the ADC will be cleared immediately.

The circuits for the Y ADC operate in an analogous manner.

In two-parameter operation, one ADC cannot be cleared before the other, as that would cause the circuits of Fig. 2 to develop an immediate RESET signal, and the data from the second ADC would be lost. Therefore, Section B of switch S1 connects the clock inputs of both clear flip-flops to the set output of the ENABLE Y flip-flop. In that case, the program must read the X-ADC first and then the Y-ADC, after which both ADC's will be cleared simultaneously.

The System Reset ($\overline{\text{SYRT}}$) line from the computer goes to ground whenever the SYSTEM RESET button on the computer console is pressed. That signal is used here to initialize the ENABLE X and ENABLE Y flip-flops to the reset state. Initialization also occurs automatically when the power is turned on.[2]

Figure 4 shows the circuits that transmit data from the ADC to the E-bus. There are 12 such circuits for each ADC, 24 in all. Each ADC data line passes to a discrete-component inverter (an IC could not withstand the voltage on the data line), which drives one input of a two-input gate. If a "one" is transmitted, that input will be low. The second input will be low when the corresponding ENABLE signal is high. The gate output will then be high and will turn on the transistor, pulling the E-bus line down.

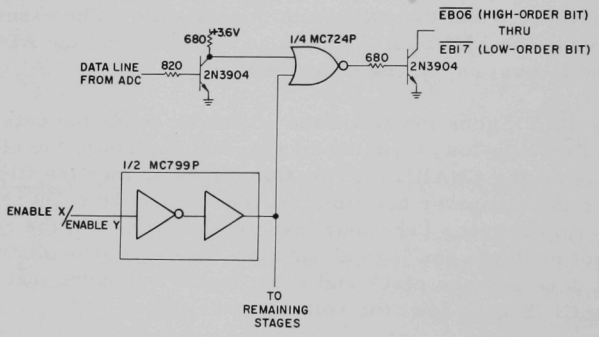

Fig. 4. ADC Interface: Data Transmission Circuits. ANL Neg. No. 116-162.

OSCILLOSCOPE INTERFACE

The oscilloscope interface develops deflection and intensification voltages to be applied to a display oscilloscope. The display oscilloscope is a Tektronix RM-564 with Type 2A60 horizontal and vertical amplifiers.

(At present, a better choice would be one of the newer CRT units designed specifically for computer display use, such as the Tektronix 601 or 611

for storage operation, or the 602 for nonstorage operation. With these units, the CRT beam-control circuits could be considerably simplified over what was needed for the 564.)

A data-output operation with the device address 55_8 generates the Y coordinate of the point to be displayed. The coordinate is specified by the high-order 12 magnitude bits of the output word, i.e., bits 5 through 16 for the 622/i, or 3 through 14 on the 620/i. (No range-switching was provided because it was assumed that the display would be scaled by programming.) Similarly, an output operation with device address 56_8 generates the X coordinate. An external-control instruction with either of the above device addresses turns on the CRT beam to display the point. The beam is turned off upon generation of a new coordinate by either of the above output instructions. If only one coordinate changes from one point to the next, only that coordinate needs to be output; the other will be held. No status sensing is necessary for this interface; it is always ready to receive data. A dummy output operation should be performed at the end of the display cycle to turn the CRT beam off.

Figure 5 shows the circuits that recognize these device addresses. If the address 55_8 appears on the E-bus in coincidence with FRYX, then $\overline{\text{SELY}}$ will be low and SELY will be high during FRYX time. If the address 56_8 appears instead, then $\overline{\text{SELX}}$ will be low and SELX will be high during FRYX time.

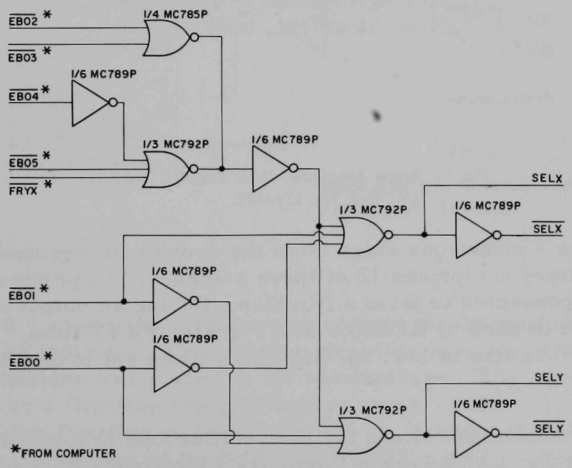

Fig. 5. Scope Interface: Selection Circuits. ANL Neg. No. 116-161.

Figure 6 shows the circuits that control the reception of coordinate data from the computer. Consider the operation for the X coordinate. The ENABLE X flip-flop is set by $\overline{\text{FRYX}}$ and reset by $\overline{\text{DRYX}}$, as described for

the ADC interface. Here, a flip-flop is primed by $\overline{\text{SELX}}$ in coincidence with E-bus line 14, which indicates an output operation. During FRYX time, the X reset signal (RESX) is high. This resets the X coordinate register to zero in preparation for receipt of the new coordinate. During DRYX time, the X strobe signal ($\overline{\text{SETX}}$) is low. This strobes the data from the E-bus into the register. The operation of the Y-coordinate circuits is analogous. (The two inverters in the set line of the ENABLE X flip-flop were provided to adjust circuit delays.)

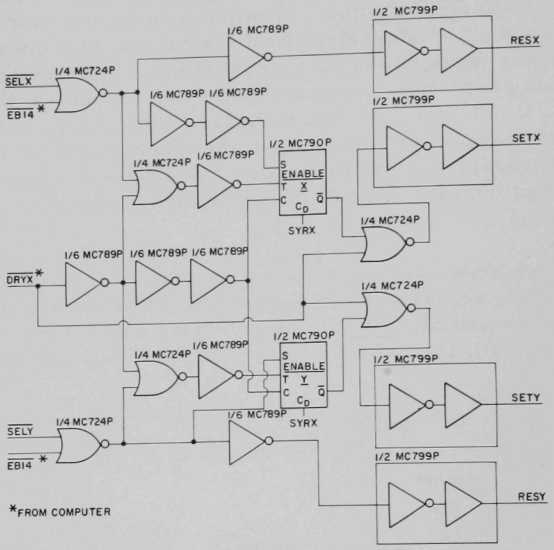

Fig. 6. Scope Interface: Data Transfer Controls.
ANL Neg. No. 116-167.

Figure 7 shows one stage from the coordinate registers. Each of the two registers comprises 12 of these stages. A stage consists of two gates cross-connected to form a flip-flop. During an output operation, the stage is reset to zero by RESX or RESY during FRYX time. Then, if the associated E-bus line is low, the flip-flop will be set to one during DRYX time.

Each deflection voltage for the oscilloscope is formed by a digital-analog converter (DAC), here a Pastoriza Electronics RSN2698. Each coordinate-register flip-flop is coupled to the DAC through a transistor stage as shown, since the flip-flop does not have enough voltage swing to drive the DAC. The output of the DAC enters the summing junction of an operational amplifier connected as a current amplifier, as shown in Fig. 8. (At present, an integrated-circuit operational amplifier would be most economical and quite suitable.) The output of this amplifier goes into the

oscilloscope. An emitter follower was included in the feedback loop to obtain enough current-output capability to drive the capacitance of the connecting cable. A zero adjustment is provided in the amplifier circuit, but display size and centering are adjusted primarily with the oscilloscope controls.

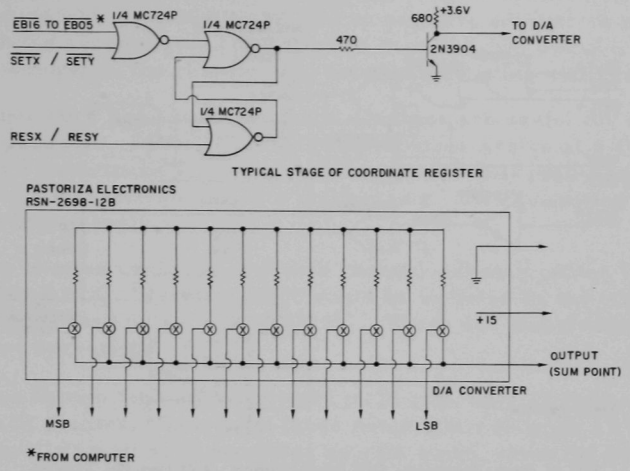

Fig. 7. Scope Interface: Coordinate Register and Digital-Analog Converter. ANL Neg. No. 116-164.

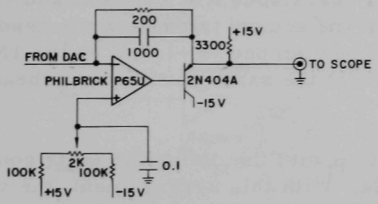

Fig. 8

Scope Interface: Coordinate Amplifier. ANL Neg. No. 116-165.

Figure 9 shows the circuits that control the intensification of the CRT beam. As indicated, some of this circuitry is in the interface chassis, while the remainder was placed in the oscilloscope. The status of the beam is controlled by a flip-flop comprising two cross-connected gates. To turn off the beam, the flip-flop is reset by an X or Y reset signal (RESX) or (RESY) or by depression of the SYSTEM RESET button. To turn on the beam, the flip-flop is set by an external-control instruction having the proper device address. (An external-control instruction is indicated by E-bus line 11 being low at FRYX time.)

With the flip-flop reset, the base and emitter of the 2N3904 NPN transistor will be at high voltage, and the 2N404A PNP transistor will be

cut off. The first triode section of the 6DJ8 will also be cut off, with its cathode held at ground by the 1N90 diode and its grid at -12.2 V. Hence, its plate, the cathode of the second triode, and one of the beam-control deflection plates in the CRT will approach +300 V. With the other deflection plate held at +125 V, the beam will be cut off.

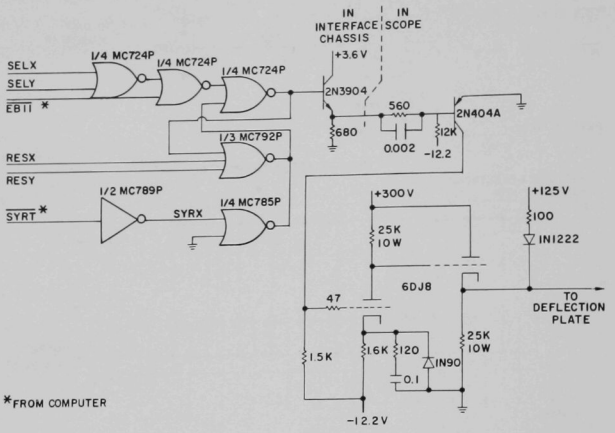

Fig. 9. Scope Interface: CRT Beam Controls. ANL Neg. No. 116-166.

With the flip-flop set, the base and emitter of the 2N3904 will be at low voltage, and the 2N404A will conduct, bringing the grid of the first triode section of the 6DJ8 to ground. That triode will conduct, and its plate voltage will fall. The cathode of the second triode and the associated deflection plate will also fall and will be clamped to +125 V by the 1N1222 diode. With both deflection plates now at the same potential, the beam is turned on.

The circuit was originally set up with the deflection plate connected directly to the plate of the first triode. With this arrangement, the voltage of the deflection plate would rise slowly after triode cutoff, because of the distributed capacitance in the circuit. As a result, the turnoff of the CRT beam would lag the resetting of the coordinate registers, producing a "tail" on the displayed point. To eliminate this, the cathode-follower was inserted to provide a low-impedance path for rapid charging of the distributed capacitance. Now, the beam turn-on is delayed by the discharge of the distributed capacitance through the cathode resistor, but this does not perturb the display.

BINARY COUNTERS

Two 17-stage binary counters are provided for use as general-purpose data-input organs. (Fifteen-stage counters would be appropriate for the 620/i.) They will count either positive or negative pulses at rates up to 4 MHz nominally (limited by the speed of the RTL circuits). Counting will stop on receipt of either a positive or negative readout-initiate pulse, after which the accumulated count may be read into the computer. After read-in is complete, the counter will reset and counting will resume.

Experience has shown that such counters are useful for a wide variety of purposes. If the readout-initiate pulses arrive at a steady rate (e.g., from a time-mark generator), the computer will read counts as a function of time in the manner of a multiscaler. Two quantities can be counted simultaneously.

The counter could also receive channel-advance pulses from a remotely located ADC. Here, readout would be initiated by the termination of the width-modulated pulse from the ADC. There are many advantages in that mode of operation.[3]

Even though the computer word is 18 bits, only 17 stages are provided in each counter. Data from these enter bits 1 through 17 in the computer. There is no point in providing an 18th stage, since bit 18 is normally interpreted as a sign bit.

Figure 10 shows the circuits that recognize the device addresses for the counters. Device address 70_8 refers to counter 1; address 71_8 refers to counter 2. If either of these addresses appears on the E-bus in coincidence with $\overline{\text{FRYX}}$, then $\overline{\text{SEL1}}$ or $\overline{\text{SEL2}}$, respectively, will become low.

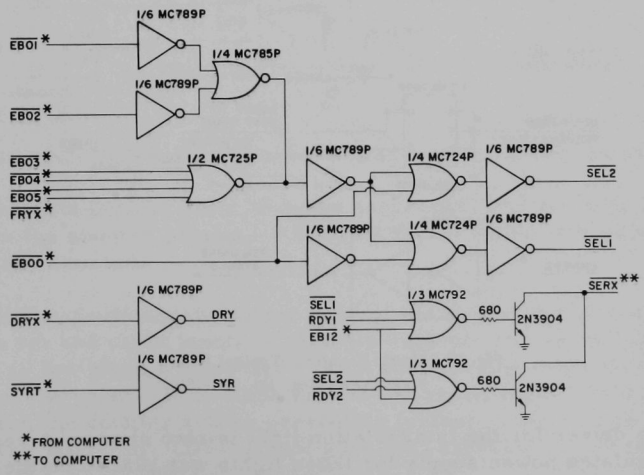

Fig. 10. Binary Counters: Selection and Ready Sensing Circuits. ANL Neg. No. 116-163.

Figure 10 also shows the ready-sensing circuits. If a counter has data ready to be read at the time a sense instruction with its device address is executed, the $\overline{\text{SERX}}$ line will be brought low, as described previously for the ADC interface.

Figure 11 shows the circuits that control data transfer from the counters to the computer. One such circuit is provided for each counter. When an input instruction with the correct device address is executed, the flip-flop is set at the end of $\overline{\text{FRYX}}$ time and reset at the end of $\overline{\text{DRYX}}$ time, as described for the previous interfaces. While the flip-flop is set, the signal EN1 or EN2, which gates the count data onto the E-bus, is formed. When the flip-flop resets, the signal RES1 or RES2 becomes high for about 0.5 μsec and resets the counter to zero.

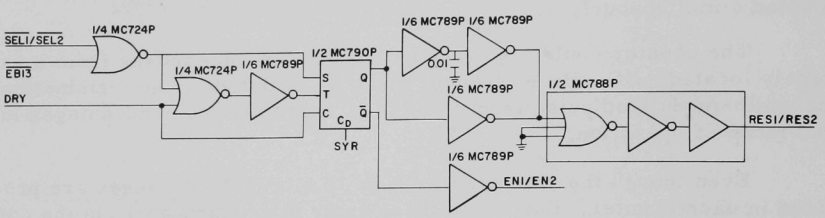

Fig. 11. Binary Counters: Data Transfer Controls. ANL Neg. No. 165-155.

Figure 12 shows one counter stage. It is simply one flip-flop connected to operate in the complementing mode. The circuit for placing data on the E-bus is also shown. The E-bus line will be pulled down if the flip-flop is in the set state when EN1 or EN2, whichever applies, is high.

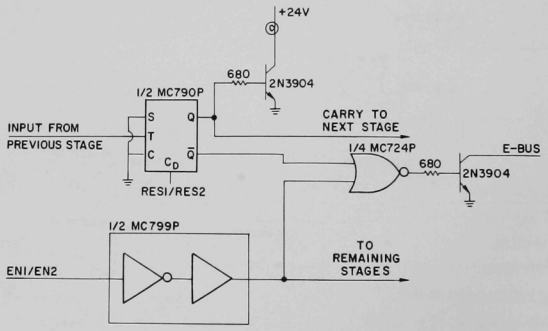

Fig. 12. Binary Counters: Typical Binary Stage. ANL Neg. No. 116-160.

The driver for the interpolation light is also shown. A separate 24-V unregulated power supply for these lights was placed on the chassis of

the 3.6-V logic power supply. In the construction, care was taken to wire the lamp grounds, i.e., the emitters of the lamp-driver transistors, separately from the logic-circuit grounds. The two ground systems were tied together at only one point. This separation minimizes logic-circuit noise resulting from voltage drops in the logic ground produced by the lamp currents.

Figure 13 shows the circuits that receive and process the data and readout-initiate pulses. Provisions are made[4] to accept either positive or negative pulses of greater than 1-V amplitude and convert them to RTL logic levels. In the quiescent state, each 2N3904 transistor will be cut off, and the inverter following it will be full on. When a pulse appears, the transistor will receive base drive and begin to conduct. When the inverter comes out of saturation, the transistor will receive additional base drive. The resulting regenerative action will rapidly turn the transistor full on and the inverter full off. When the pulse terminates, the inverse action will occur. The regenerative loop has enough hysteresis to give sharp, bounce-free transitions, even if the data pulses have very long rise and fall times.

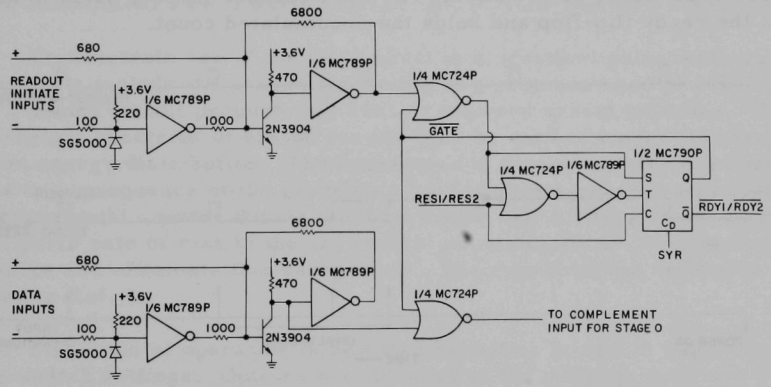

Fig. 13. Binary Counters: Data and Readout-Initiate Pulse Inputs. ANL Neg. No. 116-157.

The data pulses, after being so processed, are gated by the $\overline{\text{GATE}}$ signal into the counter proper. When that signal is low, the pulses can pass and are counted.

The readout-initiate pulses control the setting of the ready flip-flop. The set and clock inputs of that flip-flop are high in the quiescent state and go low when a pulse arrives. Thus, the flip-flop sets on the leading edge of the pulse. This takes the $\overline{\text{GATE}}$ signal high, blocking data pulses from the counter and so preventing further accumulation. Simultaneously, the $\overline{\text{RDY1}}$ or $\overline{\text{RDY2}}$ signal goes low, allowing the circuitry of

Fig. 10 to give a positive response to a sense instruction. The flip-flop remains set until the termination of data read-in, when the RES1 or RES2 pulse resets the flip-flop on its trailing edge. At this time, the counter has been reset to zero, and $\overline{\text{GATE}}$ returns low, allowing counting to resume.

When the counter is operated as a multiscaler, the readout-initiate pulses arrive at a constant rate. They are commonly derived from a time-mark generator, so that various rates may be readily selected.

Two precautions must be observed in programming for such usage. First, the program between read operations must be executed in less time than the interval between reads, so that the computer is waiting for the scaler to become ready when each readout-initiate pulse arrives. If this constraint is not observed, the process will get out of step.

In addition, the data from the first three read operations of any multiscaling sequence must be discarded. The necessity for that can be seen from the timing diagram of Fig. 14. When system power comes on, the ready flip-flop is reset by $\overline{\text{SYRT}}$, so $\overline{\text{GATE}}$ is low and whatever data pulses come along are counted. The first readout-initiate pulse to arrive sets the ready flip-flop and holds the accumulated count.

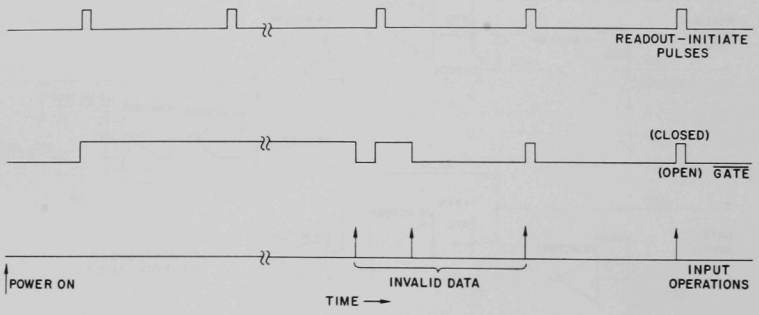

Fig. 14. Timing Diagram of Multiscaler Operation. ANL Neg. No. 116-158.

Some indeterminate time later, the first input operation is executed, which resets the counter and reopens the gate. Clearly, the count read is representative of nothing in particular and is not a valid datum.

Since the ready flip-flop was set, that input operation occurred immediately on commencement of program execution, at an arbitrary time relative to the readout-initiate pulses. Therefore, the time interval between the completion of that read operation and the next readout-initiate pulse is smaller than the normal interval, so that the datum from the next input operation would also be invalid.

There is a nonzero probability for the first input operation to occur just before a readout-initiate pulse, so the computer would not have the time to complete its processing before that pulse arrives. Thus, the ready flip-flop would not be reset until some time after the pulse, reducing the length of the next counting interval and making the subsequent input datum also invalid. This possibility can be neglected only if the processing time is very short compared with the interval between readout-initiate pulses.

Therefore, the first two and possibly the first three input operations will bring in nonvalid data, which must be discarded. This can lead to complications if the multiscaling is being done relative to an external event, such as the pulsing of a neutron generator. Proper handling of such cases will normally require additional hardware so that the event can be initiated or sensed by the computer while the multiscaling is in process. For reactor control-rod worth measurements by inverse kinetics, reading of the rod position in the second counter would fulfill the requirements if rod motion did not begin until the multiscaling process were well established.

PROGRAMMING FOR TWO-PARAMETER PULSE-HEIGHT ANALYSIS

To illustrate use of the Data-622/i in a practical pulse-analysis problem, we include the assembler listing of a program used to collect data from a proton-recoil proportional counter exposed to fast neutrons. The pulse-height spectrum of proton recoils may be used to extract the fast-neutron energy distribution. The necessity for two-parameter operation arises in consequence of the presence of a Compton electron background in the proportional counter during measurements. By forming the ratio of the initial pulse rate of rise to the asymptotic pulse amplitude, we can largely recognize and eliminate this background. The experimental method is described in Ref. 1.

The mode of operation is selected by initial A and B register and sense-switch settings. Options are included in the machine program for modes other than normal two-parameter operation. For example, each ADC may be used independently in a 128-channel full-scale single-parameter analysis useful in setup and calibration.

All modes accept pulses decoded to 512 channels maximum. In two-parameter operation, a 112-channel digital bias is set by control switches on the ADC. After a positive sense return on the appropriate X (061 device) or Y (060 device) line, the A and B registers are cleared and the data are entered by the CIA and CIB instructions.

A decrement instruction immediately follows read-in. This is done as a consequence of the practice followed by the ADC manufacturer of reserving the first channel for live-time information. A decrement deletes

the effect of the first channel without altering the linearity of any of the 100 channels used by the Y ADC in normal two-parameter operation.

For single-parameter operation, a two-bit shift right scales the spectrum to 128 channels. For two-parameter operation, the ratio of pulses (X/Y) is formed initially and scaled to 32 channels maximum, while the coincident Y pulse is scaled to 100 channels maximum. (An effective 28-channel bias exists on the Y pulse.) The 100 x 32 array, consisting of 100 energy channels and 32 ratio channels, is stored beginning at location 2000_8.

Since only the initial 2000_8 locations may be addressed directly, a faster and more efficient program results from use of the bottom of memory for the program while reserving the higher areas for data storage.

A two-parameter mode in which the 100 Y channels are summed has also been included. This mode is reached from the normal two-parameter mode by raising sense switch 1. The resulting spectrum in X/Y is scaled to 128 channels.

Various modes for survey and readout have been provided. In single-parameter modes, raising sense switch 3 causes an exit from data acquisition to oscilloscope display. The 128-channel spectrum (with intensification every 10 channels) is written repeatedly on the scope.

A scope display of the 32-channel X/Y distribution at each of the 100 Y values may also be achieved using one of the A-register control options together with a B register setting to correspond to the Y channel number.

Information in decimal form is sent to either the teletype or paper tape punch; raising sense switch 2 will select the punch. A subroutine TOUT converts binary numbers (modulus $2^{17} - 1$) into decimal form and outputs the six decimal characters. Short subroutines (PNCH, TIPE) sense the status of punch and teletype and transfer a single character to these peripherals.

Only a fraction of the basic instruction repertoire has been used in the example provided here. The intent of the program was to minimize the time involved in processing information in order to reduce the overall system deadtime and allow as high a rate of data collection as possible. Since complete address scalers and buffers exist in the ADC, digital conversion may proceed simultaneously with computer processing, and the overall system livetime was found to be high (order of 80% at a rate of order of 5000 counts per second.)

Comments at the beginning of the program are self-explanatory in listing the A-register and sense-switch options available. The first few instructions serve to interpret the A-register content in terms of a particular option chosen.

FORTRAN-COMPATIBLE SUBROUTINES FOR THE DISPLAY OSCILLOSCOPE

Machine-language subroutines are required in order to communicate with peripheral equipment from FORTRAN-compiled main programs. The basic FORTRAN library provided by the manufacturer did not contain a provision for output of data other than to the teletype and fast paper-tape system. The two subroutines (AXIS and PLOT) discussed here provide a means for writing FORTRAN-generated information on the storage scope.

AXIS traces a rectangular pattern on the scope, corresponding to the limits of the X and Y coordinates. The initial setup for the scope usually requires some adjustment of vertical and horizontal amplifier gain as well as spot intensity. This may proceed (with a pause after each trace) until sense switch 3 is raised, at which point the routine returns to the main program.

The subroutine PLOT with integer arguments IX and IY (both ranging from 0 to $2^{17} - 1$ interpreted modulo 128) causes a light spot to appear on the scope at the appropriate coordinate point. The resolution of one part in 128 is adequate for the small Tektronix scope used. The subroutine $SE (from the runtime library) plants the arguments IX and IY at the correct locations in the main program; it is required in any use of a subroutine accompanied by an argument list. After entry into the routine operation is similar to that of the analyzer program of part 1 of the appendix. A sufficient length of time must be allowed for the light spot to persist at each point in order to provide a high-quality trace.

APPENDIX

Program Listings

1. Pulse-height-analysis Program

```
*
*  NS-625 ADC WITH DATA-620/I COMPUTER PULSE HEIGHT ANALYSIS
*  FOR PROTON-RECOIL NEUTRON SPECTROSCOPY.
*  32X100 VERSION WITH EXTERNAL LIVE TIMING.
*
*  ANALYSE IN ONE-PARAMETER IF A REG. = 1(SS2 UP FOR X ADC, DOWN FOR Y
*  ANALYSE IN TWO-PARAMETER IF A REG. = 2. (SS1 FOR 1P MODE OF 2P)
*  ERASE MEMORY IF A REG. = 7
*  128 CH. SCOPE WRITE IF A = 010 (SS3 MUST BE LIT).
*  32 CH. SCOPE WRITE IF A = 020 (B REG. CONTAINS ENERGY CHANNEL).
*  PRINT OR PUNCH 128 CHANNEL SPECTRUM IF A = 0100.
*  ( IN THE 0100 READOUT MODE, THE B REGISTER IS THE START CHANNEL)
*  PUNCH FULL 3200 CHANNELS IF A = 0200 (SS2 FOR FAST PUNCH).
*
000000                    ,ORG   ,00
000000  000000      ZERO  ,HLT   ,
000001  005311            ,DAR   ,
000002  001010            ,JAZ   ,ONEP
000003  000034 R
000004  005311            ,DAR   ,
000005  001010            ,JAZ   ,TWOP
000006  000112 R
000007  006140            ,SUBI  ,5
000010  000005
000011  001010            ,JAZ   ,ERAS
000012  000217 R
000013  005311            ,DAR   ,
000014  001010            ,JAZ   ,SCOP
000015  000232 R
000016  006140            ,SUBI  ,8
000017  000010
000020  001010            ,JAZ   ,S32
000021  000345 R
000022  006140            ,SUBI  ,48
000023  000060
000024  001010            ,JAZ   ,PN1P
000025  000435 R
000026  006140            ,SUBI  ,64
000027  000100
000030  001010            ,JAZ   ,PN2P
000031  000513 R
000032  001000            ,JMP   ,ZERO  ALL ELSE RETURN
000033  000000 R
*
*  ONE PARAMETER SINGLES MODE
*
000034  001200      ONEP  ,JSS2  ,ONEX
000035  000064 R
000036  101060      ONEY  ,SEN   ,060,*+4
000037  000042 R
000040  001000            ,JMP   ,*-2
000041  000036 R
000042  102560            ,CIA   ,060   INPUT Y INTO A REG
000043  005311            ,DAR   ,
```

```
000044  004302          ,ASRA  ,2      128 CHANNELS FULL SCALE
000045  120742          ,ADD   ,IP
000046  005014          ,TAX   ,
000047  007400          ,ROF   ,
000050  045000          ,INR   ,0,1
000051  001001          ,JOF   ,OVE1   ALLOW DOUBLE PRECISION
000052  000057 R
000053  001400          ,JSS3  ,SCOP   DISPLAY WHILE SS3 LIT
000054  000232 R
000055  001000          ,JMP   ,ONEY
000056  000036 R
000057  045200     OVE1 ,INR   ,128,1
000060  005001          ,TZA   ,
000061  055000          ,STA   ,0,1
000062  001000          ,JMP   ,ONEY
000063  000036 R
*
000064  101061     ONEX ,SEN   ,061,*+4
000065  000070 R
000066  001000          ,JMP   ,*-2
000067  000064 R
000070  102561          ,CIA   ,061    INPUT X INTO A REG
000071  005311          ,DAR   ,
000072  004302          ,ASRA  ,2
000073  120742          ,ADD   ,IP
000074  005014          ,TAX   ,
000075  007400          ,ROF   ,
000076  045000          ,INR   ,0,1
000077  001001          ,JOF   ,OVE2
000100  000105 R
000101  001400          ,JSS3  ,SCOP
000102  000232 R
000103  001000          ,JMP   ,ONEX
000104  000064 R
000105  045200     OVE2 ,INR   ,128,1
000106  005001          ,TZA   ,
000107  055000          ,STA   ,0,1
000110  001000          ,JMP   ,ONEX
000111  000064 R
*
*  TWO PARAMETER NORMAL AND SINGLES MODE
*
000112  101060     TWOP ,SEN   ,060,*+4
000113  000116 R
000114  001000          ,JMP   ,*-2
000115  000112 R
000116  102661          ,CIB   ,061  INPUT X INTO B REG
000117  102560          ,CIA   ,060  INPUT Y INTO A REG
000120  005311          ,DAR   ,
000121  005322          ,DBR   ,
000122  050743          ,STA   ,Y400  STORE Y
000123  006120          ,ADDI  ,112
000124  000160
000125  050744          ,STA   ,Y512   ADD ADC BIAS AND STORE
```

```
000126  006140          ,SUBI   ,512
000127  001000
000130  001002          ,JAP    ,TWOP  IF LINEAR ADDRESS>512 BACK
000131  000112 R
000132  001100          ,JSS1   ,M21P  FOR SINGLES X/Y MODE
000133  000173 R
000134  004005          ,ASLB   ,5     MULTIPLY X BY 32
000135  005001          ,TZA    ,
000136  170744          ,DIV    ,Y512
000137  004201          ,ASLA   ,1
000140  140744          ,SUB    ,Y512
000141  001004          ,JAN    ,*+3
000142  000144 R
000143  005122          ,IBR    ,
000144  060745          ,STB    ,QUOT  DIVIDE X BY Y512 AND STORE
000145  005021          ,TBA    ,
000146  006140          ,SUBI   ,32
000147  000040
000150  001002          ,JAP    ,TWOP  IF QUOTIENT>32 GO BACK
000151  000112 R
000152  010743          ,LDA    ,Y400
000153  004302          ,ASRA   ,2     SCALE TO 100 CHANNELS
000154  004205          ,ASLA   ,5
000155  120745          ,ADD    ,QUOT   FORM SPECTRUM ADDRESS
000156  120742          ,ADD    ,IP
000157  005014          ,TAX    ,
000160  007400          ,ROF    ,
000161  045000          ,INR    ,0,1  STORE COUNT OR CORRECT
000162  001001          ,JOF    ,LAST  IF MEMORY CAPACITY EXCEEDED
000163  000166 R
000164  001000          ,JMP    ,TWOP
000165  000112 R
000166  006010     LAST ,LDAI   ,131071
000167  377777
000170  055000          ,STA    ,0,1
000171  001000          ,JMP    ,ZERO
000172  000000 R
*
*  SINGLES LOOP ON TWO PARAMETER MODE
*
000173  004007     M21P ,ASLB   ,7
000174  005001          ,TZA    ,
000175  170744          ,DIV    ,Y512
000176  060745          ,STB    ,QUOT
000177  005021          ,TBA    ,
000200  006140          ,SUBI   ,128
000201  000200
000202  001002          ,JAP    ,TWOP
000203  000112 R
000204  010745          ,LDA    ,QUOT
000205  120742          ,ADD    ,IP
000206  005014          ,TAX    ,
000207  007400          ,ROF    ,
000210  045000          ,INR    ,0,1
```

```
000211  001001          ,JOF   ,LAST
000212  000166 R
000213  001400          ,JSS3  ,SCOP  DISPLAY WHILE SS3 LIT
000214  000232 R
000215  001000          ,JMP   ,TWOP
000216  000112 R
*
*  ERASE THE MEMORY CONTAINING THE SPECTRUM
*
000217  030742     ERAS ,LDX   ,IP
000220  006020          ,LDBI  ,3200
000221  006200
000222  005001          ,TZA   ,
000223  055000          ,STA   ,0,1
000224  005322          ,DBR   ,
000225  001020          ,JBZ   ,ZERO
000226  000000 R
000227  005144          ,IXR   ,
000230  001000          ,JMP   ,*-5
000231  000223 R
*
*
*  SCOPE READOUT IN APPROPRIATE MODE
*
000232  006020     SCOP ,LDBI  ,128  READOUT OF 1P 128 CH.
000233  000200
000234  030742          ,LDX   ,IP
000235  006010          ,LDAI  ,100
000236  000144
000237  050751          ,STA   ,MAX
000240  005144     LOC1 ,IXR   ,      FIND THE MAXIMUM COUNT
000241  005322          ,DBR   ,      OR SET EQUAL TO 100.
000242  001020          ,JBZ   ,LC02
000243  000254 R
000244  015000          ,LDA   ,0,1
000245  140751          ,SUB   ,MAX
000246  001004          ,JAN   ,LOC1
000247  000240 R
000250  015000          ,LDA   ,0,1
000251  050751          ,STA   ,MAX
000252  001000          ,JMP   ,LOC1
000253  000240 R
000254  010751     LC02 ,LDA   ,MAX   PRINT MAXIMUM ON TELETYPE
000255  002000          ,CALL  ,TOUT
000256  000600 R
000257  002000          ,CALL  ,SLAS
000260  000675 R
000261  006010     LOC2 ,LDAI  ,127
000262  000177
000263  120742          ,ADD   ,IP
000264  005014          ,TAX   ,
000265  006010          ,LDAI  ,9
000266  000011
000267  050747          ,STA   ,CN10
```

```
000270  010746          ,LDA   ,SCAL
000271  050750          ,STA   ,HDEF
000272  025000     LOC3 ,LDB   ,0,1
000273  005001          ,TZA   ,
000274  160746          ,MUL   ,SCAL  SCALE Y TO MAXIMUM
000275  170751          ,DIV   ,MAX
000276  010750          ,LDA   ,HDEF
000277  103156          ,OAR   ,056   OUTPUT X AND Y TO SCOPE
000300  103255          ,OBR   ,055
000301  100056          ,EXC   ,056
000302  020747          ,LDB   ,CN10
000303  005322          ,DBR   ,       INTENSIFY EVERY 10 CHANNELS
000304  060747          ,STB   ,CN10
000305  001020          ,JBZ   ,*+4
000306  000311 R
000307  001000          ,JMP   ,*+9
000310  000320 R
000311  006020          ,LDBI  ,10
000312  000012
000313  060747          ,STB   ,CN10
000314  006020          ,LDBI  ,0200
000315  000200
000316  001000          ,JMP   ,*+4
000317  000322 R
000320  006020          ,LDBI  ,030
000321  000030
000322  005322          ,DBR   ,       DELAY TO IMPROVE TRACE
000323  001020          ,JBZ   ,*+4
000324  000327 R
000325  001000          ,JMP   ,*-3
000326  000322 R
000327  006140          ,SUBI  ,02000
000330  002000
000331  050750          ,STA   ,HDEF
000332  005344          ,DXR   ,
000333  001004          ,JAN   ,*+4
000334  000337 R
000335  001000          ,JMP   ,LOC3
000336  000272 R
000337  001400          ,JSS3  ,LOC2
000340  000261 R
000341  001100          ,JSS1  ,TWOP
000342  000112 R
000343  001000          ,JMP   ,ONEP
000344  000034 R
*
*  SCOPE DISPLAY OF A SINGLE 32 CHANNEL SPECTRUM,
*  THE B REGISTER CONTAINS THE ENERGY.
*
000345  005021     S32  ,TBA   ,
000346  004205          ,ASLA  ,5
000347  120742          ,ADD   ,IP
000350  050755          ,STA   ,AREG
000351  005014          ,TAX   ,
```

```
000352  006020          ,LDBI   ,32
000353  000040
000354  006010          ,LDAI   ,100
000355  000144
000356  05075'          ,STA    ,MAX
000357  005144      LOC4 ,IXR    ,
000360  005322          ,DBR    ,
000361  001020          ,JBZ    ,LC05
000362  000373 R
000363  015000          ,LDA    ,0,1
000364  140751          ,SUB    ,MAX
000365  001004          ,JAN    ,LOC4
000366  000357 R
000367  015000          ,LDA    ,0,1
000370  050751          ,STA    ,MAX
000371  001000          ,JMP    ,LOC4
000372  000357 R
000373  010751      LC05 ,LDA    ,MAX
000374  002000          ,CALL   ,TOUT
000375  000600 R
000376  002000          ,CALL   ,SLAS   PRINT MAX ON TELETYPE
000377  000675 R
000400  006010      LOC5 ,LDAI   ,31
000401  000037
000402  120755          ,ADD    ,AREG
000403  005014          ,TAX    ,
000404  010746          ,LDA    ,SCAL
000405  050750          ,STA    ,HDEF
000406  025000      LOC6 ,LDB    ,0,1
000407  005001          ,TZA    ,
000410  160746          ,MUL    ,SCAL   SCALE Y TO MAXIMUM
000411  170751          ,DIV    ,MAX
000412  010750          ,LDA    ,HDEF
000413  103156          ,OAR    ,056
000414  103255          ,OBR    ,055
000415  100056          ,EXC    ,056
000416  006020          ,LDBI   ,030
000417  000030
000420  005322          ,DBR    ,
000421  001020          ,JBZ    ,*+4
000422  000425 R
000423  001000          ,JMP    ,*-3
000424  000420 R
000425  006140          ,SUBI   ,010000
000426  010000
000427  050750          ,STA    ,HDEF
000430  001004          ,JAN    ,LOC5
000431  000400 R
000432  005344          ,DXR    ,
000433  001000          ,JMP    ,LOC6
000434  000406 R
*
*  PUNCH OR PRINT SPECTRA.
*  PN1P PRINTS 128 CHANNEL SPECTRA ON
```

```
*  THE TELLY, PN2P PUNCHES A FULL
*  3200 CHANNEL MATRIX ON FAST PUNCH.
*  B REG. CONTAINS THE START CHANNEL (MULTIPLES OF 32)
*
000435  005021      PN1P ,TBA   ,
000436  004205           ,ASLA  ,5
000437  120742           ,ADD   ,IP    START AT B REG.X32
000440  005014           ,TAX   ,
000441  002000           ,CALL  ,SLAS
000442  000675 R
000443  002000           ,CALL  ,SLAS
000444  000675 R
000445  002000           ,CALL  ,SLAS
000446  000675 R
000447  002000           ,CALL  ,LEDR
000450  000651 R
000451  006020           ,LDBI  ,128
000452  000200
000453  006010      WXYZ ,LDAI  ,8     EIGHT NUMBERS PER LINE
000454  000010
000455  050753           ,STA   ,LINE
000456  006010      ABCD ,LDAI  ,0240
000457  000240
000460  002000           ,CALL  ,TIPE
000461  000560 R
000462  002000           ,CALL  ,TIPE
000463  000560 R
000464  015000           ,LDA   ,0,1
000465  002000           ,CALL  ,TOUT
000466  000600 R
000467  005322           ,DBR   ,
000470  001020           ,JBZ   ,*+14
000471  000506 R
000472  005144           ,IXR   ,
000473  010753           ,LDA   ,LINE
000474  005311           ,DAR   ,
000475  050753           ,STA   ,LINE
000476  001010           ,JAZ   ,*+4
000477  000502 R
000500  001000           ,JMP   ,ABCD
000501  000456 R
000502  002000           ,CALL  ,SLAS
000503  000675 R
000504  001000           ,JMP   ,WXYZ
000505  000453 R
000506  002000           ,CALL  ,SLAS
000507  000675 R
000510  002000           ,CALL  ,LEDR
000511  000651 R
000512  000000           ,HLT   ,
*
*
000513  001200      PN2P ,JSS2  ,*+6
000514  000521 R
```

```
000515  006010          ,LDAI   ,0222
000516  000222
000517  002000          ,CALL   ,TIPE
000520  000560 R
000521  002000          ,CALL   ,LEDR
000522  000651 R
000523  006020          ,LDBI   ,3200
000524  006200
000525  030742          ,LDX    ,IP
000526  006010      PP2 ,LDAI   ,32
000527  000040
000530  050753          ,STA    ,LINE
000531  015000      PP1 ,LDA    ,0,1
000532  002000          ,CALL   ,TOUT
000533  000600 R
000534  005322          ,DBR    ,
000535  001020          ,JBZ    ,*+14
000536  000553 R
000537  005144          ,IXR    ,
000540  010753          ,LDA    ,LINE
000541  005311          ,DAR    ,
000542  050753          ,STA    ,LINE
000543  001010          ,JAZ    ,*+4
000544  000547 R
000545  001000          ,JMP    ,PP1
000546  000531 R
000547  002000          ,CALL   ,SLAS
000550  000675 R
000551  001000          ,JMP    ,PP2
000552  000526 R
000553  002000          ,CALL   ,SLAS
000554  000675 R
000555  002000          ,CALL   ,LEDR
000556  000651 R
000557  000000          ,HLT    ,
*
*
*LIST OF SUBROUTINES
*
*TIPE SUBROUTINE. OUTPUT SYMBOL TO TELLY
*
000560  000000     TIPE ,ENTR   ,
000561  101101          ,SEN    ,0101,*+4
000562  000565 R
000563  001000          ,JMP    ,*-2
000564  000561 R
000565  103101          ,OAR    ,01
000566  001000          ,RETU*  ,TIPE
000567  100560 R
*
*  PNCH SUBROUTINE. OUTPUTS SYMBOL TO FAST PUNCH.
*
000570  000000     PNCH ,ENTR   ,
000571  101537          ,SEN    ,0537,*+4
```

```
000572  000575 R
000573  001000          ,JMP    ,*-2
000574  000571 R
000575  103137          ,OAR    ,037
000576  001000          ,RETU*  ,PNCH
000577  100570 R
*
*  TOUT SUBROUTINE. OUTPUTS A 6-DIGIT NUMBER TO FAST PUNCH
*  IF SS2 LIT, OTHERWISE TO TELLY.
*
000600  000000      TOUT ,ENTR   ,
000601  060756           ,STB    ,BREG
000602  070757           ,STX    ,XREG
000603  050754           ,STA    ,NUMB
000604  006010           ,LDAI   ,100000
000605  303240
000606  050752           ,STA    ,DEC
000607  005004      JP4  ,TZX    ,
000610  010754           ,LDA    ,NUMB
000611  140752      JP2  ,SUB    ,DEC
000612  001004           ,JAN    ,JP1
000613  000617 R
000614  005144           ,IXR    ,
000615  001000           ,JMP    ,JP2
000616  000611 R
000617  120752      JP1  ,ADD    ,DEC
000620  050754           ,STA    ,NUMB
000621  005041           ,TXA    ,
000622  006120           ,ADDI   ,0260
000623  000260
000624  001200           ,JSS2   ,*+6
000625  000632 R
000626  002000           ,CALL   ,TIPE
000627  000560 R
000630  001000           ,JMP    ,*+4
000631  000634 R
000632  002000           ,CALL   ,PNCH
000633  000570 R
000634  020752           ,LDB    ,DEC
000635  005001           ,TZA    ,
000636  006170           ,DIVI   ,10
000637  000012
000640  001020           ,JBZ    ,JP3
000641  000645 R
000642  060752           ,STB    ,DEC
000643  001000           ,JMP    ,JP4
000644  000607 R
000645  020756      JP3  ,LDB    ,BREG
000646  030757           ,LDX    ,XREG
000647  001000           ,RETU*  ,TOUT
000650  100600 R
*
*  LEDR SUBROUTINE. PUNCHES LEADER.
*
```

```
000651  000000      LEDR ,ENTR  ,
000652  006020           ,LDBI  ,60
000653  000074
000654  006010           ,LDAI  ,0200
000655  000200
000656  001200           ,JSS2  ,*+6
000657  000664 R
000660  002000           ,CALL  ,TIPE
000661  000560 R
000662  001000           ,JMP   ,*+4
000663  000666 R
000664  002000           ,CALL  ,PNCH
000665  000570 R
000666  005322           ,DBR   ,
000667  001020           ,JBZ   ,*+4
000670  000673 R
000671  001000           ,JMP   ,*-11
000672  000656 R
000673  001000           ,RETU* ,LEDR
000674  100651 R
*
*  SLAS ROUTINE TERMINATES RECORDS SAME AS FORTRAN.
*
000675  000000       SLAS,ENTR  ,
000676  006010           ,LDAI  ,0215
000677  000215
000700  001200           ,JSS2  ,DOWN
000701  000722 R
000702  002000           ,CALL  ,TIPE
000703  000560 R
000704  006010           ,LDAI  ,0377
000705  000377
000706  002000           ,CALL  ,TIPE
000707  000560 R
000710  006010           ,LDAI  ,0212
000711  000212
000712  002000           ,CALL  ,TIPE
000713  000560 R
000714  006010           ,LDAI  ,0377
000715  000377
000716  002000           ,CALL  ,TIPE
000717  000560 R
000720  001000           ,RETU* ,SLAS
000721  100675 R
000722  002000       DOWN,CALL  ,PNCH
000723  000570 R
000724  006010           ,LDAI  ,0377
000725  000377
000726  002000           ,CALL  ,PNCH
000727  000570 R
000730  006010           ,LDAI  ,0212
000731  000212
000732  002000           ,CALL  ,PNCH
000733  000570 R
```

```
000734  006010          ,LDAI   ,0377
000735  000377
000736  002000          ,CALL   ,PNCH
000737  000570 R
000740  001000          ,RETU*  ,SLAS
000741  100675 R
*
*  IDENTIFY VARIABLES.
*
000742  002000        IP,DATA   ,02000  START OF DATA ARRAY
000743  000000      Y400,DATA   ,0
000744  000000      Y512,DATA   ,0
000745  000000      QUOT,DATA   ,0
000746  377777      SCAL,DATA   ,0377777   FULL SCALE TO D-A CONVERTER
000747  000000      CN10,DATA   ,0
000750  000000      HDEF,DATA   ,0
000751  000000       MAX,DATA   ,0
000752  000000       DEC,DATA   ,0
000753  000000      LINE,DATA   ,0
000754  000000      NUMB,DATA   ,0
000755  000000      AREG,DATA   ,0
000756  000000      BREG,DATA   ,0
000757  000000      XREG,DATA   ,0
*
        000000          ,END    ,

LITERALS

POINTERS


SYMBOLS

1  000757 R  XREG          1  000526 R  PP2
1  000756 R  BREG          1  000513 R  PN2P
1  000755 R  AREG          1  000456 R  ABCD
1  000754 R  NUMB          1  000453 R  WXYZ
1  000753 R  LINE          1  000435 R  PN1P
1  000752 R  DEC           1  000406 R  LOC6
1  000751 R  MAX           1  000400 R  LOC5
1  000750 R  HDEF          1  000373 R  LC05
1  000747 R  CN10          1  000357 R  LOC4
1  000746 R  SCAL          1  000345 R  S32
1  000745 R  QUOT          1  000272 R  LOC3
1  000744 R  Y512          1  000261 R  LOC2
1  000743 R  Y400          1  000254 R  LC02
1  000742 R  IP            1  000240 R  LOC1
1  000722 R  DOWN          1  000232 R  SCOP
1  000675 R  SLAS          1  000217 R  ERAS
1  000651 R  LEDR          1  000173 R  M21P
1  000645 R  JP3           1  000166 R  LAST
1  000617 R  JP1           1  000112 R  TWOP
1  000611 R  JP2           1  000105 R  OVE2
1  000607 R  JP4           1  000064 R  ONEX
1  000600 R  TOUT          1  000057 R  OVE1
1  000570 R  PNCH          1  000036 R  ONEY
1  000560 R  TIPE          1  000034 R  ONEP
1  000531 R  PP1           1  000000 R  ZERO
```

2. Subroutine AXIS

```
*   FORTRAN COMPATIBLE ASSEMBLY.
*
*   AXIS SUBROUTINE. PLOTS AXIS UNTIL SS3 LIT, THEN PLOTS
*   THREE MARKS AND TERMINATES. A HALT IS GIVEN AFTER COMPLETING
*   THE RECTANGLE TO ALLOW A MANUAL SCOPE ERASE.
*
          000000 R          ,FORT   ,
          000000 R          ,NAME   ,AXIS
000000    000000      AXIS  ,ENTR   ,
000001    054114            ,STA    ,AREG
000002    064114            ,STB    ,BREG    SAVE REGISTERS
000003    074114            ,STX    ,XREG
000004    006010      STRT  ,LDAI   ,0377777
000005    377777
000006    005002            ,TZB    ,
000007    002000            ,CALL   ,SPHO
000010    000121 R
000011    006140            ,SUBI   ,02000
000012    002000
000013    001004            ,JAN    ,*+4
000014    000017 R
000015    001000            ,JMP    ,*-6
000016    000007 R
000017    006010            ,LDAI   ,0377777     MAKE HORIZONTAL LINES
000020    377777
000021    005012            ,TAB    ,
000022    002000            ,CALL   ,SPHO
000023    000121 R
000024    006140            ,SUBI   ,02000
000025    002000
000026    001004            ,JAN    ,*+4
000027    000032 R
000030    001000            ,JMP    ,*-6
000031    000022 R
000032    006010            ,LDAI   ,0377777
000033    377777
000034    005002            ,TZB    ,
000035    002000            ,CALL   ,SPVE
000036    000140 R
000037    006140            ,SUBI   ,02000       MAKE VERTICAL LINES
000040    002000
000041    001004            ,JAN    ,*+4
000042    000045 R
000043    001000            ,JMP    ,*-6
000044    000035 R
000045    006010            ,LDAI   ,0377777
000046    377777
000047    005012            ,TAB    ,
000050    002000            ,CALL   ,SPVE
000051    000140 R
000052    006140            ,SUBI   ,02000
000053    002000
000054    001004            ,JAN    ,*+4
000055    000060 R
```

```
000056  001000          ,JMP    ,*-6
000057  000050 R
000060  000000          ,HLT    ,
000061  001400          ,JSS3   ,*+4     IF SS3 DRAW MARKS
000062  000065 R
000063  001000          ,JMP    ,STRT      OR ERASE SCOPE AND RE-TRACE.
000064  000004 R
000065  006020          ,LDBI   ,0277777
000066  277777
000067  006010      BACK ,LDAI  ,010000
000070  010000
000071  002000          ,CALL   ,SPVE
000072  000140 R
000073  006140          ,SUBI   ,02000
000074  002000
000075  001004          ,JAN    ,*+4
000076  000101 R
000077  001000          ,JMP    ,*-6
000100  000071 R
000101  005021          ,TBA    ,
000102  006140          ,SUBI   ,0100000
000103  100000
000104  001004          ,JAN    ,*+5
000105  000111 R
000106  005012          ,TAB    ,
000107  001000          ,JMP    ,BACK
000110  000067 R
000111  014004          ,LDA    ,AREG    RETURN REGISTERS
000112  024004          ,LDB    ,BREG
000113  034004          ,LDX    ,XREG
000114  001000          ,RETU*  ,AXIS
000115  100000 R
000116  000000      AREG ,DATA  ,0
000117  000000      BREG ,DATA  ,0
000120  000000      XREG ,DATA  ,0
000121  000000      SPHO ,ENTR  ,        FOR HORIZONTAL LINES
000122  103156          ,OAR    ,056
000123  103255          ,OBR    ,055
000124  100056          ,EXC    ,056
000125  006030          ,LDXI   ,010000
000126  010000
000127  005344          ,DXR    ,
000130  001040          ,JXZ    ,*+4
000131  000134 R
000132  001000          ,JMP    ,*-3
000133  000127 R
000134  103156          ,OAR    ,056     TURN OFF SPOT
000135  103255          ,OBR    ,055
000136  001000          ,RETU*  ,SPHO
000137  100121 R
000140  000000      SPVE ,ENTR  ,        FOR VERTICAL LINES
000141  103155          ,OAR    ,055
000142  103256          ,OBR    ,056
000143  100056          ,EXC    ,056
```

```
000144   006030          ,LDXI   ,010000
000145   010000
000146   005344          ,DXR    ,
000147   001040          ,JXZ    ,*+4
000150   000153 R
000151   001000          ,JMP    ,*-3
000152   000146 R
000153   103155          ,OAR    ,055    TURN OFF SPOT
000154   103256          ,OBR    ,056
000155   001000          ,RETU*  ,SPVE
000156   100140 R
         000000          ,END    ,
```

SYMBOLS

```
1  000140 R  SPVE
1  000121 R  SPHO
1  000120 R  XREG
1  000117 R  BREG
1  000116 R  AREG
1  000067 R  BACK
1  000004 R  STRT
1  000000 R  AXIS
```

3. Subroutine PLOT

```
*   FORTRAN COMPATIBLE ASSEMBLY.
*
*   PLOT SUBROUTINE.  PLOTS IX AND IY ON SCOPE.
*   IX AND IY ARE SINGLE-PRECISION NUMBERS MODULUS 2 TO THE 17.
*
          000000 R          ,FORT   ,
          000000 R          ,NAME   ,PLOT
          000000 E    $SE   ,EXT    ,
000000    000000      PLOT  ,ENTR   ,
000001    002000            ,CALL   ,$SE,2,0,0
000002    000000 E
000003    000002
000004    000000
000005    000000
000006    054031            ,STA    ,AREG     SAVE REGISTERS
000007    064031            ,STB    ,BREG
000010    074031            ,STX    ,XREG
000011    006037            ,LDXE   ,PLOT+4
000012    000004 R
000013    015000            ,LDA    ,0,1       IX PLACED IN A REGISTER
000014    006037            ,LDXE   ,PLOT+5
000015    000005 R
000016    025000            ,LDB    ,0,1       IY PLACED IN B REGISTER
000017    103156            ,OAR    ,056      OUTPUT IX TO X
000020    103255            ,OBR    ,055      OUTPUT IY TO Y
000021    100056            ,EXC    ,056      TURN ON SPOT
000022    006030            ,LDXI   ,010000
000023    010000
000024    005344            ,DXR    ,          DELAY FOR SPOT QUALITY
000025    001040            ,JXZ    ,*+4
000026    000031 R
000027    001000            ,JMP    ,*-3
000030    000024 R
000031    103156            ,OAR    ,056     TURN OFF SPOT
000032    103255            ,OBR    ,055
000033    014004            ,LDA    ,AREG     RETURN REGISTERS
000034    024004            ,LDB    ,BREG
000035    034004            ,LDX    ,XREG
000036    001000            ,RETU*  ,PLOT
000037    100000 R
000040    000000      AREG  ,DATA   ,0
000041    000000      BREG  ,DATA   ,0
000042    000000      XREG  ,DATA   ,0
          000000            ,END    ,
```

SYMBOLS

```
1  000042 R  XREG
1  000041 R  BREG
1  000040 R  AREG
1  000000 R  PLOT
1  000000 E  $SE
```

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